Logic

74AXPnT245 – transceiver

Quad dual supply translating transceiver; 3-state

Design benefit

- Translating transceiver for wide voltage ranges.
- Low static and dynamic power consumption for portable applications.
- I_{off} circuitry provides power-down mode operation
- Specified from -40 °C to 125 °C

Key technical features & portfolio

- New portfolio with 4-bit & 8-bit dual supply transceivers
- Wide supply voltage offers from 0.9V to 5.5V
- Small footprint packages for both TSSOP and DHVQFN

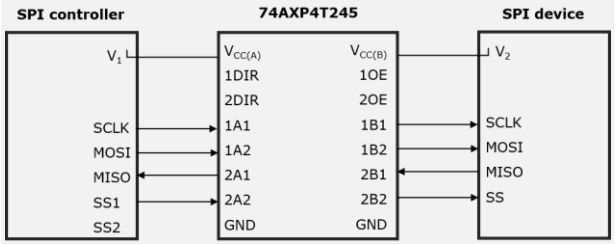
Portfolio	$V_{CC(A)}$ & $V_{CC(B)}$	I_{CC}	Package
74AXP4T245PW	0.9V – 5.5V	24µA	TSSOP16
74AXP4T245BQ	0.9V – 5.5V	24µA	DHVQFN16
74AXP8T245PW	0.9V – 5.5V	35µA	TSSOP24
74AXP8T245BQ	0.9V – 5.5V	35µA	DHVQFN24

Functions & applications

- Industrial applications
- General portable consumer applications
- Enterprise and Telecom applications

Application diagram

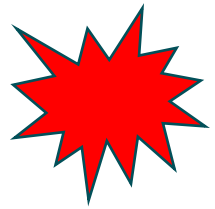
SPI interface application



Available packages (W x L x H in mm)

PW (SOD403-1)	BQ (SOD763-1)
	
5 x 4.4 x 1.1	3.5 x 2.5 x 1.0

PW (SOD355-1)	BQ (SOD815-1)
	
7.8 x 4.4 x 2.0	5.5 x 3.5 x 1.0



Logic

GX4 MicroPak

4 pad, low power gates

Design benefit

- X2SON4 MicroPak provide the industry's smallest footprint for logic plastic packages
- with a pad spacing ≥0.4mm no step-down stencil required - enables low cost board manufacturing
- RoHS and dark-green compliant with NiPdAu lead finish
- Low profile height of 0.35mm

Key technical features & portfolio

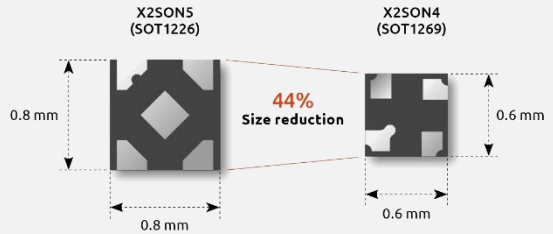
- AUP and LVC families offer
  - 1G34GX4: Buffer
  - 1G17GX4: Buffer Schmitt-trigger
  - 1G07GX4: Buffer with open-drain
  - 1G04GX4: Inverter
  - 1G14GX4: Inverter Schmitt-trigger
- Propagation delay
  - AUP1G: t_{pd} 4.0ns (V_{cc} 1.8V, C_L 15pF)
  - LVC1G: t_{pd} 2.0ns (V_{cc} 2.5V, C_L 50pF)
- Static current 0.01µA for LVC1G and 0.1µA for AUP1G

Portfolio	Voltage	Max. Output	Temperature Range
LVC1G	1.65-5.5V	± 32mA	−40 to +125 °C
AUP1G	0.8-3.6V	± 4mA	−40 to +125 °C

Functions & applications

- Space constrained applications such as smartphones, tablets and portables
- Communication and industrial applications

Package advantage



Available packages (W x L x H in mm)

GX4 (SOT1296-2)

0.6 x 0.6 x 0.32

Logic

74AVC1T8xxx Qualcomm

Single dual-supply translating 2-input OR or NOR with strobe

Design benefit

- Low cost alternative solution for Qualcomm's reference board design.
- Wide supply voltage range
  - ✓ $V_{CC(A)}$: 0.8 V to 3.6 V
  - ✓ $V_{CC(B)}$: 0.8 V to 3.6 V
- Supports mixed-mode voltage operations
- Maximum data rates:
  - ✓ 500 Mbit/s(1.8V to 3.3V translation)
  - ✓ 320 Mbit/s(translate to 2.5V or 1.8V)

Key technical features & portfolio

- Over-voltage tolerant inputs, accepts voltages up to 3.6V
- I_{OFF} circuitry provides partial power down operation
- Inputs with Schmitt trigger action
- Suspend mode
- High noise immunity

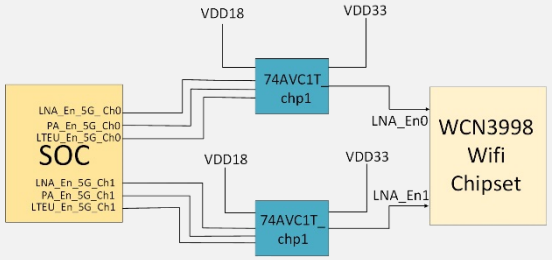
Portfolio	$V_{CC(A)}$ & $V_{CC(B)}$	Output Current	Prop del (t_{PD})	T_{amb}
74AVC1T8832GS	0.8 – 3.6V	+/-12mA	2.4ns	-40~125°C
74AVC1T8128GS	0.8 – 3.6V	+/-12mA	2.4ns	-40~125°C

Functions & applications

- Wireless module
- Mobile / Portable applications
- Industrial applications

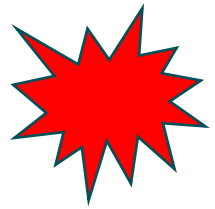
Application diagram

- Example of voltage translation between the MCU and a WIFI chipset on different voltage rails



Available packages (W x L x H in mm)

Package name	XSON8
	
pin count	8
version	SOT833-1
suffix	GT
Pitch (mm)	0.50
W x L x H (mm)	1.0 x 1.95 x 0.50



Logic

LV-A logic Family

Low leakage family for partial power down by I_{OFF} circuit

Design benefit

- I_{OFF} circuitry supports partial power-down
- Low noise operation: VOL(p) < 0.8 V
- Fully specified at 3.3 V and 5.0 V supply nodes
- overvoltage tolerant inputs support mixed-mode voltage
- Schmitt-trigger inputs for slowly transitioning input signals
- Latch-up performance exceeds 250 mA
- ESD - HBM exceeds 3 kV (ANSI/ESDA/JEDEC JS-001, Class 2)

Key technical features & portfolio

- I_{OFF} power down
- Low noise
- 3.3V and 5V supply voltage support
- Translater function

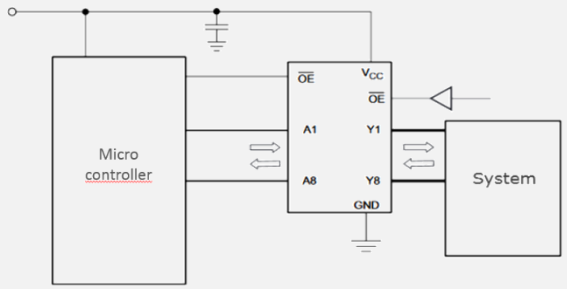
Part number	Portfolio size	features
74LVxxxAxx	8 parts	Inverter, buffer, transceiver, OVT, CMOS inputs
74LVxxxATxx	5 parts	Inverter, buffer, transceiver, OVT, TTL inputs
74AHCVxxxAxx	6 parts	Inverter, buffer, transceiver, OVT, Schmitt trigger inputs
74AHCTxxxAxx	7 parts	Inverter, buffer, transceiver, OVT, TTL inputs

Functions & applications

- The LV-A family is designed to support applications where in different modes e.g. stand-by mode a part of the PCB is shut down. Applications:
- Printer
- TV sets
- Desktop and notebook computer

Application diagram

- Example of voltage translation between MCU and system rail at different voltage



Available packages

Package name	TSSOP	TSSOP
		
Pin count	14	20
version	SOT402-1	SOT360-1
suffix	PW	PW
Pitch (mm)	0.65	0.65
W x L x H (mm)	6.4 x 5.0 x 1.1	6.4 x 6.5 x 1.1

Autosense translators NXB/NXS

On roadmap

A family of 1-8 bit bidirectional level shifter and voltage translator with auto direction sensing

Design benefit

- Two completely separate power lines may be used
- translates logic voltage levels with auto direction sensing
- versions for open-drain (NXB) and push-pull CMOS logic (NXS) output
- Pb-free, RoHS and dark green compliant
- specified for partial power-down applications using I_{OFF}
- Automotive version on roadmap

Key technical features & portfolio

- voltages: $V_{CC(A)}$= 1.65 V to 3.6 V; $V_{CC(B)}$= 2.3 V to 5.5 V
- Maximum data rates: 26 Mbps (Push-pull)
- Inputs accept voltages up to 5.5 V
- Latch-up performance <100 mA per JESD 78B Class II

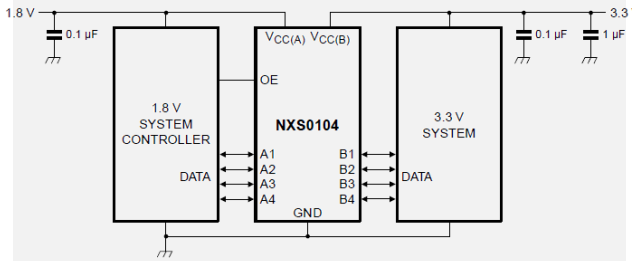
Part number		Portfolio size	packages
NXx0101xx	1 bit	6	GM= XSON6 (SOT886), GS= XSON6 (SOT1202), GW= TSSOP6 (SOT363-1)
NXx0102xx	2 bit	4	GT= XSON8 (SOT833-1) DC= VSSOP8 (SOT765-1)
NXx0104xx	4 bit	6	GU12= XQFN12 (SOT1174-1) BQ= DQFN14 (SOT762-1) PW= TSSOP14 (SOT402-1)
NXx0108xx	8 bit	4	BQ= DQFN20 (SOT764-1) PW= TSSOP20 (SOT360-1)

Functions & applications

- Mobile application like smartphone, wearables
- Computing application like notebook, tablet, desktop PC
- Industrial application
- Automotive applications (on roadmap)

Application diagram

- Example of voltage translation between 1.8V MCU and 3.3V system rail



Available packages (selection)

Package name	XSON6	XSON8	XQFN12
			
pin count	6	8	12
Version	SOT1202	SOT833-1	SOT1174-1
Suffix	GS	GT	GU12
Pitch (mm)	0.35	0.50	0.40
W x L x H (mm)	1.0 x 1.0 x 0.35	1.0 x 1.95 x 0.50	2.0 x 1.7 x 0.50

Logic

MicroPak packages AEC-Q100 qualified

Automotive qualified

Automotive qualified Mini logic in leadless packages

Design benefit

- Optimized for speed and power
- Low propagation delay
- Low dynamic power dissipation
- Pb-free, RoHS and dark green compliant
- specified for partial power-down applications using I_{OFF}

Key technical features & portfolio

- Very small footprint - up to 65% space saving over traditional leaded packages
- pin pitch options: 0.5, 0.35 mm
- Low profile height: 0.5 or 0.35 mm
- Leadless - no bent leads, no co-planarity issues
- Pb-free, RoHS and dark green compliant

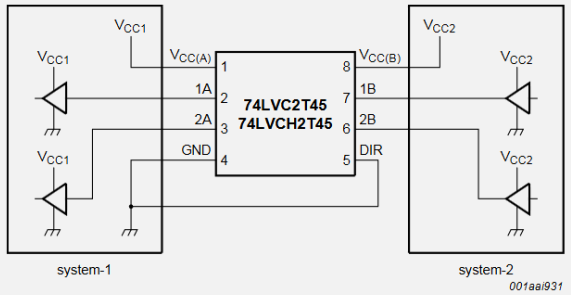
Part number	Types	Features
74AUPxxxxxGx-Q100	7	Gates, Inverter, buffer, voltage translator, multiplexer, OVT, CMOS or Schmitt trigger inputs
74AVC1T45GS-Q100	1	single bit, dual supply transceiver, bidirectional level translation
74LVCxxxxxGx-Q100	14	Gates, Inverter, buffer, voltage translator, multiplexer, OVT, CMOS or Schmitt trigger inputs

Functions & applications

- space constraint automotive applications e.g.:
- Infotainment
- ADAS
- BMS

Application diagram

- Example of uni-directional logic level-shifting translation



Available packages (selection)

Package name	XSON6	XSON6	XSON8
			
pin count	6	6	8
version	SOT1202	SOT886	SOT833-1
suffix	GS	GM	GT
Pitch (mm)	0.35	0.50	0.50
W x L x H (mm)	1.0 x 1.0 x 0.35	1.0 x 1.45 x 0.50	1.0 x 1.95 x 0.50

Logic

EFFICIENCY WINS.